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12179-P098US

PATENT



- 1 -

BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re Application: Iwamatsu

Serial No.: 09/836,857

Filed: April 17, 2001

Art Unit: 2881

Examiner: David Vanore

For: ELECTRON BEAM DUPLICATION LITHOGRAPHY  
METHOD AND APPARATUS

Mail Stop AF  
Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

**APPEAL BRIEF**

I. REAL PARTY-IN-INTEREST

The real party in interest is SI Diamond Technology, Inc., who is the assignee of the entire right and interest in the present Application.

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**CERTIFICATION UNDER 37 C.F.R. § 1.8**

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to Mail Stop AF, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on 9-14, 2004.

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165.00 OP

Signature

Toni Stanley

(Printed name of person certifying)

## II. RELATED APPEALS AND INTERFERENCES

There are no appeals or interferences known to Appellants, the Appellants' legal representative, or assignee which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

## III. STATUS OF CLAIMS

Claims 1-9 and 15-20 are pending in the Application, and also stand rejected.

## IV. STATUS OF AMENDMENTS

There were no amendments to the claims or Specification filed after the final rejection.

## V. SUMMARY OF THE INVENTION

The present invention provides an electron beam duplication lithography apparatus and method (FIG. 1) for focusing electrons is emitted from a mask plate 10 as a result of an application of an electric field between a mask plate 10 and a duplication plate 13. Page 7, line 14- page 8, line 16. The result is that a congruent or similar pattern is lithographed by electron beam exposure onto an electron beam resist film 14 from a field emission film 12 having the congruent or similar pattern to be created. Page 9, lines 9-18.

Because there is no use of a photo cathode, it is possible to realize a longer lifetime of the mask plate 10. Moreover, it is possible to construct the mask plate 10 using a conductive substrate 11 or having a conductive film coated glass substrate or ceramic substrate or a metal substrate, at a lower cost. Moreover, it is possible to achieve higher current densities with a field emitter 12, resulting in a lessening of the

exposure time of the resist film 14, resulting in a faster lithography process, which will increase the manufacturing throughput.

Because the mask plate 10 surface is flat, it is possible to more effectively duplicate in a one-to-one manner, plus there is no inherent limit to the size of the cathode. The whole pattern can be exposed in parts of it at a time. It is also possible to realize more precise duplication lithography below the 0.1 micrometer level.

A field emission device can use low work function materials, such as a diamond-like carbon thin film. As a result, the two plates 10, 13 can be positioned closer together resulting in higher current densities, resulting in the increased efficiency, all without a degradation of the mask plate 10, since the diamond-like carbon thin film 12 is more resistant to damage over its lifetime.

#### VI. REJECTIONS

1. Claims 15-19 stand rejected under 35 U.S.C. § 112, first paragraph, as failing to comply with the written description requirement.

2. Claims 1-4, 6, 9, and 20 stand rejected under 35 U.S.C. § 102(b) as being clearly anticipated by *Baylor et al.* (USP 5,892,231).

3. Claim 5 stands rejected under 35 U.S.C. § 103 as being unpatentable over *Baylor* in view of *Park* (USP 5,743,998).

4. Claims 7-8 stand rejected under 35 U.S.C. § 103 as being unpatentable over *Baylor*.

VII. ARGUMENT

1. Claims 15-19 are not properly rejected under 35 U.S.C. § 112, first paragraph.

## A. General

On pages 4-5 of the Final Rejection, the Examiner has merely made a blanket statement that the negative limitations recited in claims 15-19 constitute new matter and are not supported by the original disclosure. However, in accordance with MPEP § 2163.04, the Examiner has not met the required burden of proof with such a rejection. The Examiner has the initial burden of presenting by a preponderance of evidence why a person skilled in the art would not recognize in an applicant's disclosure a description of the invention defined by the claims. The Examiner has provided no evidence in support of his assertions. Therefore, for this reason alone, his *prima facie* case of a § 112 rejection must fail. In rejecting a claim, the Examiner must set forth express findings of fact which support the lack of written description conclusion, including establishing a *prima facie* case by providing reasons why a person skilled in the art at the time the application was filed would not have recognized that the inventor was in possession of the invention as claimed in view of the disclosure of the application as filed.

## B. Claim 15

Claim 15 specifically recites that when the electric field is established there is no deactivated field emission material. This claim limitation is supported by the drawings and the Specification. FIGURE 1 shows an apparatus of the present invention where plural patterned field emission devices 12 emitted electrons towards the electron beam resist film 14 upon application of the electric field between the

mask plate 10 and the duplicated plate 13. *See Specification*, page 8, lines 4-11. FIGURE 2 shows an exemplary duplicated plate 21 with pattern 22 where the resist material 14 of FIGURE 1 has been patterned by electron beam lithography from an electron field emission device 12, which has the same pattern as the pattern 22 shown in FIGURE 2. *See Specification*, page 9, lines 9-15. Page 10, lines 1-3 describes how such a process can be performed in a very short period of time, such as 10 milliseconds. No undue experimentation is needed by one skilled in the art to realize that the pattern 22 was created by the field emitters 12 having the same pattern, and that all of these field emitters 12 shown in FIGURE 1 were activated at the same time, and that none of them were deactivated. Thus, claim 15 is adequately supported.

C. Claim 16

Claim 16 recites that it is not possible to deactivate selected portions of the field emission material. This claim limitation is quite clearly supported by the Specification, since there is nothing with the Specification or the drawings that show that any of the field emitters 12 can be deactivated when the device shown in FIGURE 1 is enabled with a power supply putting an electric field between plates 10 and 13. Again, no undue experimentation would be needed by one skilled in the art to implement this claimed invention in view of the disclosure.

D. Claim 17

Claim 17 recites that deactivation of selected portions of the field emission material is not required to define the predefined pattern. The pattern created in the resist film 14, and as shown in FIGURE 2, does not require a deactivation of selected portions of the field emission material 12. In other words, the pattern 22 created on duplicated plate 21 is a result of all of the field emitters 12 being activated having a similar pattern. *See Specification*, page 9, lines 13-15.

## E. Claim 18

Claim 18 recites that the field emitter is not matrix addressable. It is clear from the Specification and FIGURE 1 that the field emitter 12 is not matrix addressable. The electrode of the power supply is connected to substrate 11 activating each and every one of the field emitters 12.

## F. Claim 19

Claim 19 recites that the electron beam resist layer is not modified in the spaces between the predefined pattern since no field emission of electrons occurs in such spaces. FIGURE 1 clearly shows that the electron beam resist film 14 is a solid film over all of substrate 13 and that there is no modification of any part of such layer 14. One skilled in the art would not be required to perform any undue experimentation in order to arrive at the claimed invention.

2. Claims 1-4, 6, 9 and 20 are not properly rejected under 35 U.S.C. § 102(b) as being clearly anticipated by *Baylor*.

## A. Claim 1

Claim 1 recites that all of the field emission material deposited on the first substrate in the predefined pattern on a permanent basis emits electrons on a continuous basis when activated. The Examiner asserts that when a current is applied to the emitters 431-434 in *Baylor*, they continuously emit electrons. Applicants respectfully disagree. The device in *Baylor* is a digitally addressable array of electron emitters configurable in a variety of shapes so that when a particular shape of an electron beam is desired, selected ones of the electron emitters will be activated to create such desired shape. In such a case, there will be certain ones of the electron emitters that are not activated. So, for example, the *Baylor* invention of FIGURE 5 overcomes the prior art shown in FIGURE 3 of *Baylor* whereby if a T design is desired, the square-shaped electron beam will have to be repeated for various portions

of the T design. With the *Baylor* invention, only the emitters 431-434 making up the T design will be activated so that the entire T design can be emitted as an electron beam in that shape. In such a case, there will be electron emitters that are not activated in *Baylor*. Claim 1 recites that all of the field emission material will emit electrons on a continuous basis when activated. This is not taught within *Baylor*, since *Baylor* teaches that not all of the field emitters will be addressed to emit electrons, but instead, some of them will not be activated to define the desired pattern.

On page 2 of the Final Rejection, the Examiner has traversed Applicant's assertions regarding the teachings of *Baylor*, however, Applicants do not understand what the Examiner is attempting to state. Applicants have asserted that the *Baylor* field emitter array will have field emitters not activated, while the present invention has all of its emitters activated. Claim 1 recites that all of the field emission material is activated by the electric field. It actually seems that the Examiner is agreeing with Applicants in his response to Arguments. It would frustrate the purpose of *Baylor* for the *Baylor* device to be able activate all of its emitters, since it would not accomplish the patterning taught by the *Baylor* invention.

#### B. Claim 4

With respect to claim 4, the Examiner has asserted in the Final Rejection that since the item 520 in *Baylor* must be able to conduct an electrical signal, it is therefore necessarily conductive in nature. This is simply taking the teachings of the prior art and interpreting the present invention out of context. It is also an unreasonable interpretation of the claim language. Though an Examiner may broadly interpret claim language, such an interpretation must be reasonable and consistent with the interpretation that those skilled in the art would reach. MPEP § 2111. One skilled in the art would not interpret the conductive layer recited within claim 4 as being the same as a logic and memory circuit 520 to control an emitter as taught in *Baylor*.

## Claim 6

With respect to claim 6, the grids 441-444 are not deposited on the substrate 510. Claim 6 recites a conductive or dielectric material deposited on the first substrate between portions of the patterned field emitter. The Examiner believes that a reasonable and ordinary meaning to the word "on" includes something that is not necessarily in contact with the other object. The Examiner asserts that since a "book on a table" is a "book on the earth" since the "table is on the earth," then the grids are deposited on the substrate 510. First, the Examiner is not taking into consideration all of the language recited within claim 6. Claim 6 recites that the conductive or dielectric material is deposited on the first substrate. If one were to say that a book is deposited on a table they would not then say that it is also deposited on the earth. One skilled in the art would take the reasonable interpretation of deposited on the table as being that it is actually in contact with the table and is not on the earth. One skilled in the art of creating such circuitry would clearly understand that stating that something is deposited on a substrate means that that object is in contact with the substrate as a result of the deposition of the material on the substrate. Thus, Applicants respectfully assert that the Examiner's interpretation of the claim language is unreasonable. MPEP § 2111. Secondly, the table and earth analogy does not adequately support the Examiner's position. No one goes around stating that objects are on the earth, except possibly an astronomer or a NASA scientist. Only one skilled in the art of space exploration would talk in such a manner. One skilled in the art in producing semiconductor devices would not talk in such a manner. Because the Examiner's table and earth analogy is so preposterous, it cannot in any way be a reasonable interpretation.



## D. Claim 20

With respect to claim 20, since again item 520 in *Baylor* is not a conductive layer, and one skilled in the art would not have reasonably interpreted it to be a conductive layer, *Baylor* does not meet the claim limitation of the conductive or dielectric material being in contact with the first substrate.

3. Claim 5 is not properly rejected under 35 U.S.C. § 103 as being unpatentable over *Baylor* in view of *Park*.

Claim 5 recites that the establishing circuitry further comprises a conductive layer between the second substrate and the electron beam resist layer. The Examiner admits that *Baylor* does not teach this limitation, but asserts that *Park* does. The Examiner cites to column 2, lines 3-28 of *Park*. The problem with the Examiner's assertion is that there is no substrate disclosed in *Park* in col. 2, lines 3-28. There is merely a resist media deposited on the conductive layer. Thus, *Park* only teaches two layers, while the present invention, as recited in claim 5 recites three layers, the resist layer, the conductive layer, and the substrate. The Examiner then responds that layer 6 in Figs. 1A-1C is a substrate. True, but layer 4 is a processing layer, not a conductive layer.

4. Claims 7 and 8 are not properly rejected under 35 U.S.C. § 103 as being unpatentable over *Baylor*.

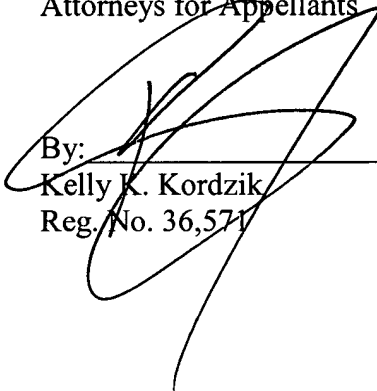
Claim 7 recites that the conductive or dielectric material covers edges of the field emitter. Claim 8 recites that the surface of the conductive or dielectric material is co-planar with an emitting surface of the field emitter. The Examiner merely cites language in *Baylor* that it is within the level of ordinary skill in the art to provide emitters and grid elements of any shape so long as a suitable emitting field is produced. However, this language does not teach or suggest a conductive or dielectric material covering edges of the field emitter that is recited in claims 1 and 6,

nor does this language teach or suggest a surface of the conductive or dielectric material is co-planar with an emitting surface of the field emitter. One skilled in the art at the time the invention was made would not have been able to recreate these inventions as specifically recited within these claims in view of a broad statement that emitters and grid elements can be any shape. The Examiner is essentially just asserting that claims 7 and 8 would have been obvious without any objective support for his assertions. These limitations are not found within the art cited by the Examiner, and thus the Examiner has not proven a *prima facie* case of obviousness in rejecting these claims.

Respectfully submitted,

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APPENDIX

1           1. An electron beam duplication lithography apparatus comprising:  
2           a first substrate;  
3           a field emitter deposited on the first substrate in a predefined pattern whereby  
4           an active field emission material is deposited on the first substrate in the predefined  
5           pattern on a permanent basis such that all of such field emission material emits  
6           electrons on a continuous basis when activated, and whereby no active field emission  
7           material resides in spaces between the predefined pattern so that no field emission of  
8           electrons occurs in such spaces;  
9           a second substrate positioned a distance from the first substrate;  
10          an electron beam resist layer deposited on the second substrate; and  
11          circuitry for establishing an electric field to thereby cause an emission of  
12          electron beams from the active field emission material towards the electron beam  
13          resist layer in order to modify the electron beam resist layer in a pattern substantially  
14          identical to the predefined pattern.

1           2. The apparatus as recited in claim 1, further comprising a magnetic field  
2           lens positioned to focus the electron beams as they are emitted from the field emitter  
3           towards the electron beam resist layer.

1           3. The apparatus as recited in claim 1, further comprising an electric field lens  
2           positioned to focus the electron beams as they are emitted from the field emitter  
3           towards the electron beam resist layer.

1           4. The apparatus as recited in claim 1, wherein the establishing circuitry  
2           further comprises a conductive layer between the first substrate and the field emitter.

1           5. The apparatus as recited in claim 1, wherein the establishing circuitry  
2 further comprises a conductive layer between the second substrate and the electron  
3 beam resist layer.

1           6. The apparatus as recited in claim 1, further comprising a conductive or  
2 dielectric material deposited on the first substrate between portions of the patterned  
3 field emitter.

1           7. The apparatus as recited in claim 6, wherein the conductive or dielectric  
2 material covers edges of the field emitter

1           8. The apparatus as recited in claim 6, wherein a surface of the conductive or  
2 dielectric material is coplanar with a emitting surface of the field emitter.

1           9. The apparatus as recited in claim 6, wherein an emitting surface of the field  
2 emitter is recessed below a surface of the conductive or dielectric material.

1           15. The apparatus as recited in claim 1, wherein when the electric field is  
2 established there is no de-activated field emission material.

1           16. The apparatus as recited in claim 1, wherein it is not possible to de-  
2 activate selected portions of the field emission material.

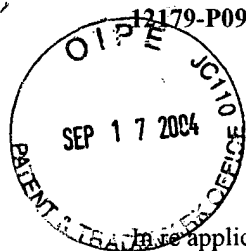
1           17. The apparatus as recited in claim 1, wherein de-activation of selected  
2 portions of the field emission material is not required to define the predefined pattern.

1           18. The apparatus as recited in claim 1, wherein the field emitter is not  
2 matrix-addressable.

1           19. The apparatus as recited in claim 1, wherein the electron beam resist layer  
2 is not modified in the spaces between the predefined pattern since no field emission  
3 of electrons occurs in such spaces.

1           20. The apparatus as recited in claim 6, wherein the conductive or dielectric  
2 material is in contact with the first substrate.

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12179-P098US 9/14/2004



12179-P098US

PATENT

## IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: Iwamatsu

Serial No.: 09/836,857 Art Unit: 2881  
Filed: April 17, 2001 Examiner: David Vanore  
For: ELECTRON BEAM DUPLICATION LITHOGRAPHY METHOD AND APPARATUS

Mail Stop Appeal Brief - Patents

Commissioner for Patents

P.O. Box 1450

Alexandria, VA 22313-1450

**TRANSMITTAL OF APPEAL BRIEF**  
**(PATENT APPLICATION - 37 CFR 1.192)**

1. Transmitted herewith in triplicate is the APPEAL BRIEF in this application with respect to the Notice of Appeal filed on July 15, 2004.

NOTE: "The appellant shall, within 2 months from the date of the notice of appeal under § 1.191 in an application, reissue application, or patent under reexamination, or within the time allowed for response to the action appealed from, if such time is later, file a brief in triplicate." 37 CFR 1.192(a) (emphasis added).

## 2. STATUS OF APPLICANT

This application is on behalf of

☐ other than a small entity☒ small entity

## 3. FEE FOR FILING APPEAL BRIEF

Pursuant to 37 CFR 1.17(f) the fee for filing the Appeal Brief is:

☒ small entity \$165.00☐ other than a small entity \$330.00

Appeal Brief fee due \$165.00

**CERTIFICATE OF MAILING (37 CFR § 1.8)**

I hereby certify that this paper (along with any paper referred to as being attached or enclosed) is being deposited with the United States Postal Service on the date shown below with sufficient postage as first class mail in an envelope addressed to Mail Stop Appeal Brief - Patents, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

Date: 9-14-04

Toni Stanley

(Type or print name of person mailing paper)

Toni Stanley

(Signature of person mailing paper)

(Page 1 of 3)

**4. EXTENSION OF TERM**

*NOTE: The time periods set forth in 37 CFR 1.192(a) are subject to the provision of § 1.136 for patent applications. 37 CFR 1.191(d). Also see Notice of November 5, 1985 (1060 O.G. 27).*

The proceedings herein are for a patent application and the provisions of 37 CFR 1.136 apply.

*(complete (a) or (b) as applicable)*

- (a) ☐ Applicants petition for an extension of time under 37 CFR 1.136 (fees: 37 CFR 1.17(a)-(d)) for the total number of months checked below:

Extension (months)	Fee for other than small entity	Fee for small entity
<input type="checkbox"/> one month	\$ 110.00	\$ 55.00
<input type="checkbox"/> two months	\$ 420.00	\$ 210.00
<input type="checkbox"/> three months	\$ 950.00	\$ 475.00
<input type="checkbox"/> four months	\$ 1,480.00	\$ 740.00
Fee		\$ _____

If an additional extension of time is required, please consider this a petition therefor.

*(check and complete the next item, if applicable)*

- ☐ An extension for \_\_\_\_\_ months has already been secured and the fee paid therefor of \$ \_\_\_\_\_ is deducted from the total fee due for the total months of extension now requested.

Extension fee due with this request \$ \_\_\_\_\_

or

- (b) ☒ Applicants believe that no extension of term is required. However, this conditional petition is being made to provide for the possibility that applicants have inadvertently overlooked the need for a petition and fee for extension of time.

**5. TOTAL FEE DUE**

The total fee due is:

Appeal Brief fee \$165.00

Extension fee (if any) \$0.00

**TOTAL FEE DUE \$165.00**

**6. FEE PAYMENT**

- ☒ Attached is a check in the sum of \$ 165.00

- ☐ Charge Account No. \_\_\_\_\_ the sum of \$ 0.

**A duplicate of this transmittal is attached.**

**7. FEE DEFICIENCY**

*NOTE: If there is a fee deficiency and there is no authorization to charge an account, additional fees are necessary to cover the additional time consumed in making up the original deficiency. If the maximum, six-month period has expired before the deficiency is noted and corrected, the application is held abandoned. In those instances where authorization to charge is included, processing delays are encountered in returning the papers to the PTO Finance Branch in order to apply these charges prior to action on the cases. Authorization to charge the deposit account for any fee deficiency should be checked. See the Notice of April 7, 1986, 1065 O.G. 31-33.*

- ☒ If any additional extension and/or fee is required, this is a request therefor and to charge Account No. 23-2426 (12179-P098US).

AND/OR

- ☒ If any additional fee for claims is required, charge Account No. 23-2426 (12179-P098US).

Reg. No.: 36,571

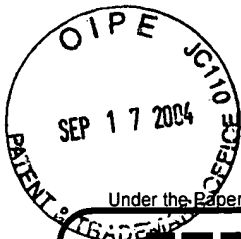
  
SIGNATURE OF ATTORNEY

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12179-P098US 9/14/2004





PTO/SB/17 (10-03)

Approved for use through 07/31/2006. OMB 0651-0032  
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

# FEE TRANSMITTAL for FY 2004

Effective 10/01/2003. Patent fees are subject to annual revision.

☒ Applicant claims small entity status. See 37 CFR 1.27

TOTAL AMOUNT OF PAYMENT (\$ 165.00

**Complete if Known**

Application Number	09/836,857
Filing Date	4/17/2001
First Named Inventor	Iwamatsu
Examiner Name	David Vanore
Art Unit	2881
Attorney Docket No.	12179-P098US

**METHOD OF PAYMENT** (check all that apply)☒ Check ☐ Credit card ☐ Money Order ☐ Other ☐ None☒ Deposit Account:Deposit Account Number: 23-2426  
Deposit Account Name: Winstead Sechrest & Minick P.C.

The Director is authorized to: (check all that apply)

☐ Charge fee(s) indicated below ☒ Credit any overpayments☒ Charge any additional fee(s) or any underpayment of fee(s)☐ Charge fee(s) indicated below, except for the filing fee to the above-identified deposit account.**FEE CALCULATION****1. BASIC FILING FEE**

Large Entity Fee Code (\$)	Small Entity Fee Code (\$)	Fee Description	Fee Paid
1001 770	2001 385	Utility filing fee	
1002 340	2002 170	Design filing fee	
1003 530	2003 265	Plant filing fee	
1004 770	2004 385	Reissue filing fee	
1005 160	2005 80	Provisional filing fee	
SUBTOTAL (1)			(\$ 0

**2. EXTRA CLAIM FEES FOR UTILITY AND REISSUE**

Total Claims	Extra Claims	Fee from below	Fee Paid
0	-20** = 0	18	0
0	-3** = 0	86	0
0		0	0

Large Entity Fee Code (\$)	Small Entity Fee Code (\$)	Fee Description
1202 18	2202 9	Claims in excess of 20
1201 86	2201 43	Independent claims in excess of 3
1203 290	2203 145	Multiple dependent claim, if not paid
1204 86	2204 43	** Reissue independent claims over original patent
1205 18	2205 9	** Reissue claims in excess of 20 and over original patent

SUBTOTAL (2) (\$ 0

\*\*or number previously paid, if greater. For Reissues, see above

**FEE CALCULATION** (continued)**3. ADDITIONAL FEES**

Large Entity Small Entity

Fee Code (\$)	Fee Code (\$)	Fee Description	Fee Paid
1051 130	2051 65	Surcharge - late filing fee or oath	
1052 50	2052 25	Surcharge - late provisional filing fee or cover sheet	
1053 130	1053 130	Non-English specification	
1812 2,520	1812 2,520	For filing a request for <i>ex parte</i> reexamination	
1804 920*	1804 920*	Requesting publication of SIR prior to Examiner action	
1805 1,840*	1805 1,840*	Requesting publication of SIR after Examiner action	
1251 110	2251 55	Extension for reply within first month	
1252 420	2252 210	Extension for reply within second month	
1253 950	2253 475	Extension for reply within third month	
1254 1,480	2254 740	Extension for reply within fourth month	
1255 2,010	2255 1,005	Extension for reply within fifth month	
1401 330	2401 165	Notice of Appeal	165
1402 330	2402 165	Filing a brief in support of an appeal	
1403 290	2403 145	Request for oral hearing	
1451 1,510	1451 1,510	Petition to institute a public use proceeding	
1452 110	2452 55	Petition to revive - unavoidable	
1453 1,330	2453 665	Petition to revive - unintentional	
1501 1,330	2501 665	Utility issue fee (or reissue)	
1502 480	2502 240	Design issue fee	
1503 640	2503 320	Plant issue fee	
1460 130	1460 130	Petitions to the Commissioner	
1807 50	1807 50	Processing fee under 37 CFR 1.17(q)	
1806 180	1806 180	Submission of Information Disclosure Stmt	
8021 40	8021 40	Recording each patent assignment per property (times number of properties)	
1809 770	2809 385	Filing a submission after final rejection (37 CFR 1.129(a))	
1810 770	2810 385	For each additional invention to be examined (37 CFR 1.129(b))	
1801 770	2801 385	Request for Continued Examination (RCE)	
1802 900	1802 900	Request for expedited examination of a design application	

Other fee (specify)

\*Reduced by Basic Filing Fee Paid

SUBTOTAL (3) (\$ 165

**SUBMITTED BY**

(Complete if applicable)

Name (Print/Type)	Kelly K. Kordzik	Registration No. (Attorney/Agent)	36,571	Telephone	512-370-2851
Signature		Date	9-14-04		

**WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.**

This collection of information is required by 37 CFR 1.17 and 1.27. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

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